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PRODUCT OVERVIEW

SAM88RCRI PRODUCT FAMILY

Samsung's SAM88RCRI family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes.

A address/data bus architecture and a large number of bit-configurable I/O ports provide a flexible programming environment for applications with varied memory and I/O requirements. Timer/counters with selectable operating modes are included to support real-time operations.

S3C9442/C9444/C9452/C9454 MICROCONTROLLER

The S3C9442/C9444/C9452/C9454 single-chip 8-bit microcontroller is designed for useful A/D converter , SIO application field. The S3C9442/C9444/C9452/C9454 uses powerful SAM88RCRI CPU and S3C9442/C9444/C9452/C9454 architecture. The internal register file is logically expanded to increase the on-chip register space.

The S3C9442/C9444/C9452/C9454 has 2K/4K bytes of on-chip program ROM and 208 bytes of RAM. The S3C9442/C9444/C9452/C9454 is a versatile general-purpose microcontroller that is ideal for use in a wide range of electronics applications requiring simple timer/counter, PWM. In addition, the S3C9442/C9444/C9452/C9454's advanced CMOS technology provides for low power consumption and wide operating voltage range.

Using the SAM88RCRI design approach, the following peripherals were integrated with the SAM88RCRI core:

- Three configurable I/O ports (18 pins)
- Four interrupt sources with one vector and one interrupt level
- One 8-bit timer/counter with time interval mode
- Analog to digital converter with nine input channels and 10-bit resolution
- One 8-bit PWM output

The S3C9442/C9444/C9452/C9454 microcontroller is ideal for use in a wide range of electronic applications requiring simple timer/counter, PWM, ADC. S3C9452/C9454 is available in a 20/16-pin DIP and a 20-pin SOP package. S3C9452/C9454 is available in a 8-pin and a 8-pin SOP package.

MTP

The S3F9444/F9454 is an MTP (Multi Time Programmable) version of the S3C9442/C9444/C9452/C9454 microcontroller. The S3F9444/F9454 has on-chip 4-Kbyte multi-time programmable flash ROM instead of masked ROM. The S3F9444/F9454 is fully compatible with the S3C9442/C9444/C9452/C9454, in function, in D.C. electrical characteristics and in pin configuration.

FEATURES

CPU

- SAM88RCRI CPU core
- The SAM88RCRI core is low-end version of the current SAM87 core.

Memory

- 2/4-Kbyte internal program memory
- 208-byte general purpose register area

Instruction Set

- 41 instructions
- The SAM88RCRI core provides all the SAM87 core instruction except the word-oriented instruction, multiplication, division, and some one-byte instruction.

Instruction Execution Time

- 400 ns at 10 MHz f_{OSC} (minimum)

Interrupts

- 4 interrupt sources with one vector
- One interrupt level

General I/O

- Three I/O ports (Max 18 pins)
- Bit programmable ports

8-bit High-speed PWM

- 8-bit PWM 1-ch (Max: 156 kHz)
- 6-bit base + 2-bit extension

Built-in reset Circuit

- Low voltage detector for safe reset

Timer/Counters

- One 8-bit basic timer for watchdog function
- One 8-bit timer/counter with time interval modes

A/D Converter

- Nine analog input pins
- 10-bit conversion resolution

Oscillation Frequency

- 1 MHz to 10 MHz external crystal oscillator
- Maximum 10 MHz CPU clock
- Internal RC: 3.2 MHz (typ.), 0.5 MHz (typ.) in $V_{DD} = 5\text{ V}$

Operating Temperature Range

- -40°C to $+85^{\circ}\text{C}$

Operating Voltage Range

- 2.0 V (LVR Level) to 5.5 V

Smart Option

Package Types

- S3C9452/C9454:
 - 20-DIP-300A
 - 20-SOP-375
 - 16-DIP-300A
- S3C9442/C9444
 - 8-DIP-300
 - 8-SOP-225

BLOCK DIAGRAM

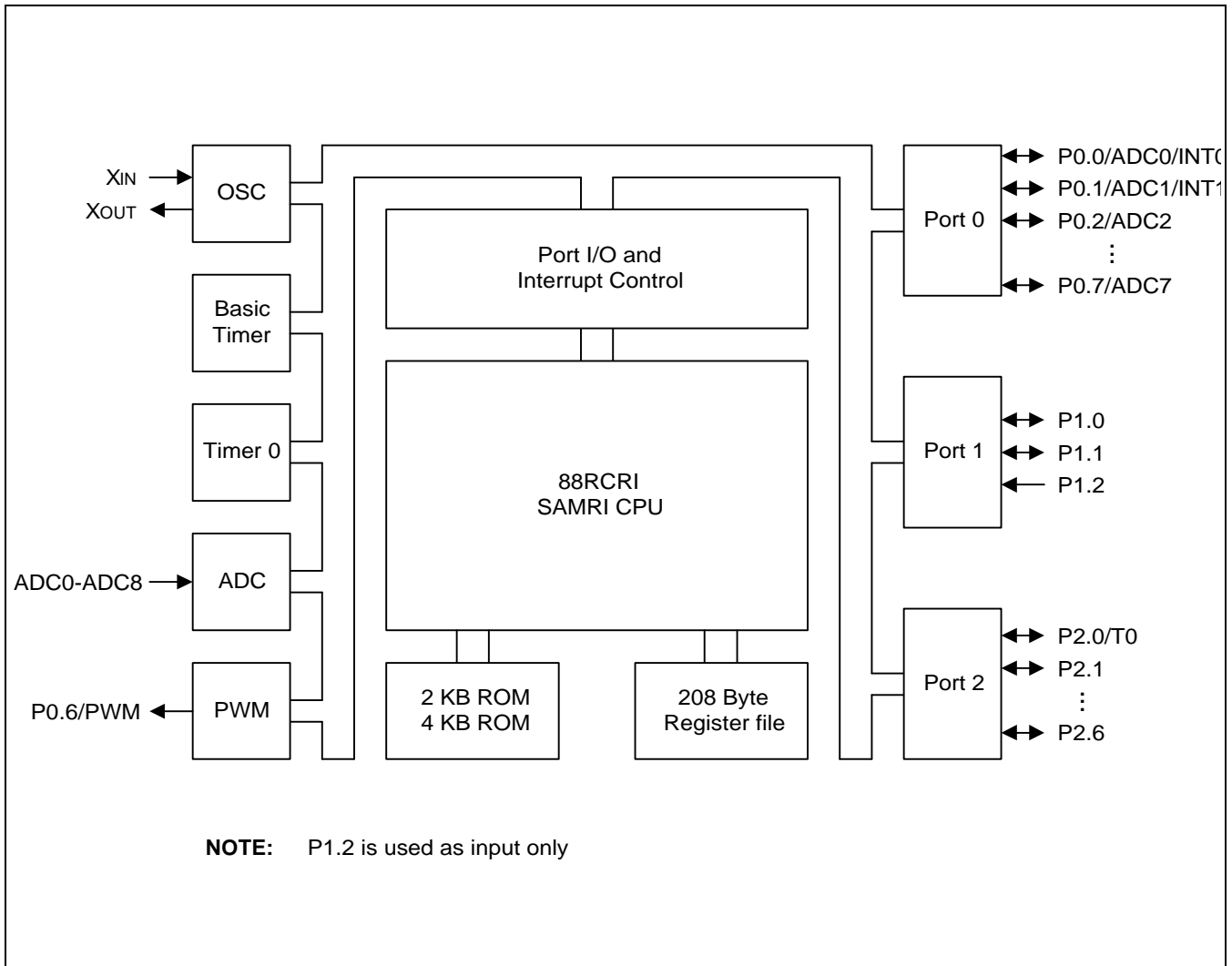


Figure 1-1. Block Diagram

PIN ASSIGNMENTS

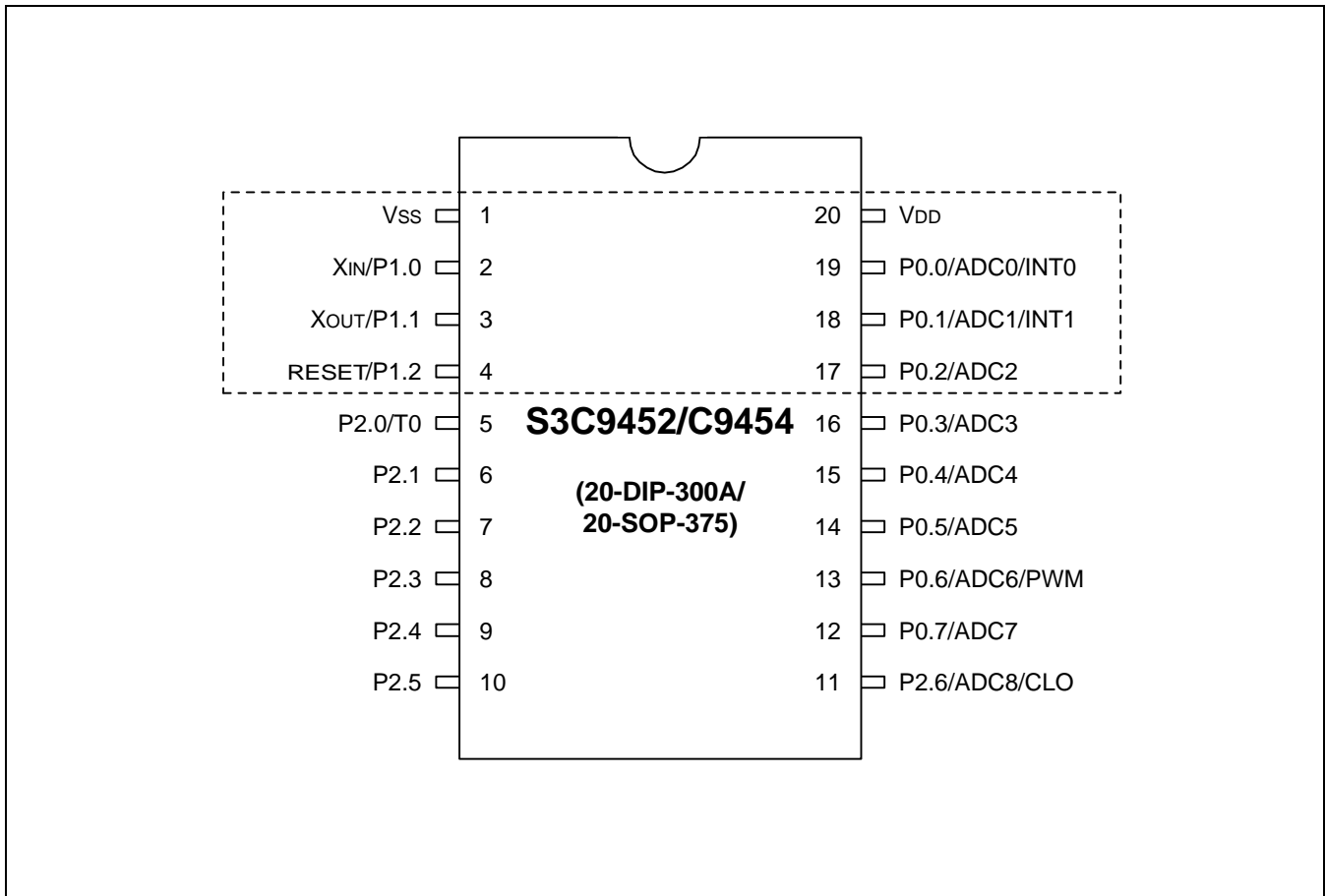


Figure 1-2. Pin Assignment Diagram (20-Pin DIP/SOP Package)

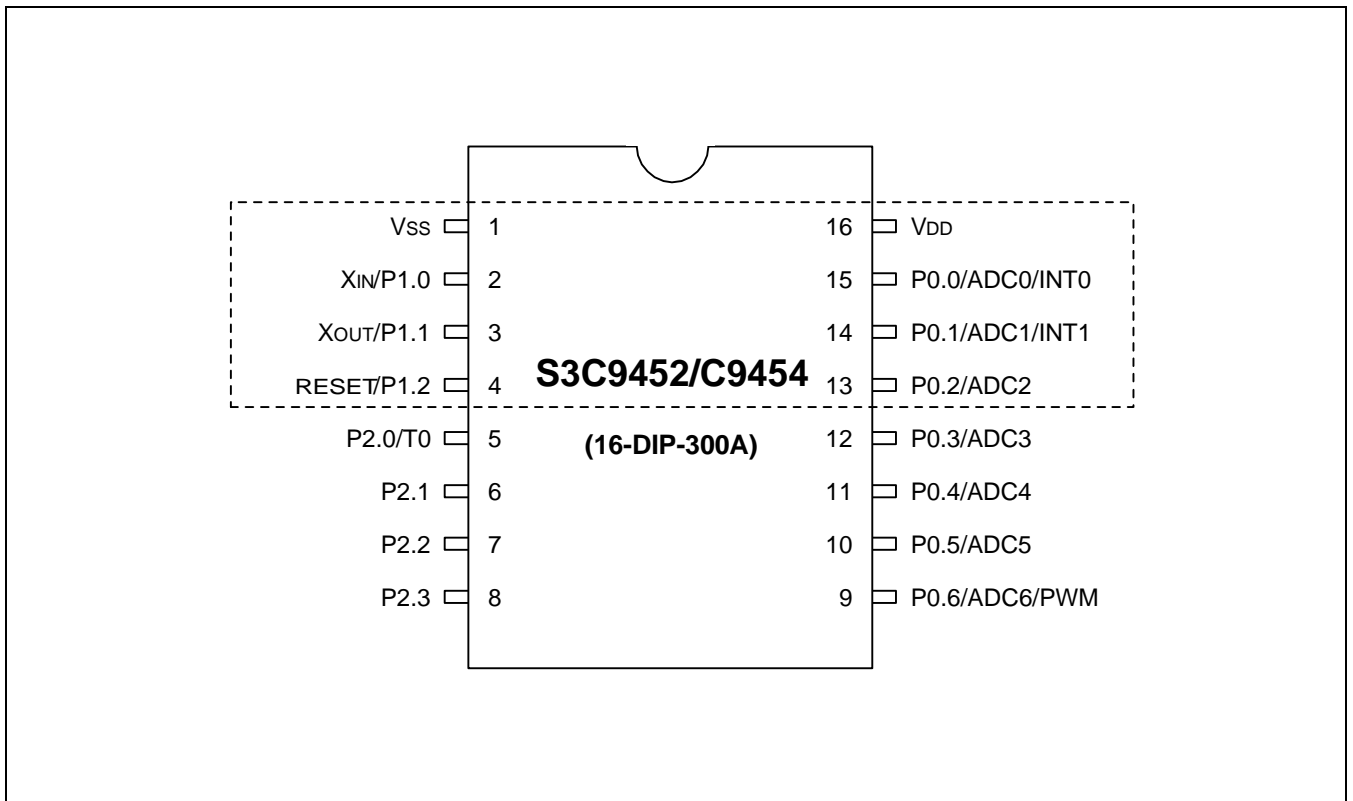


Figure 1-3. Pin Assignment Diagram (16-Pin DIP Package)

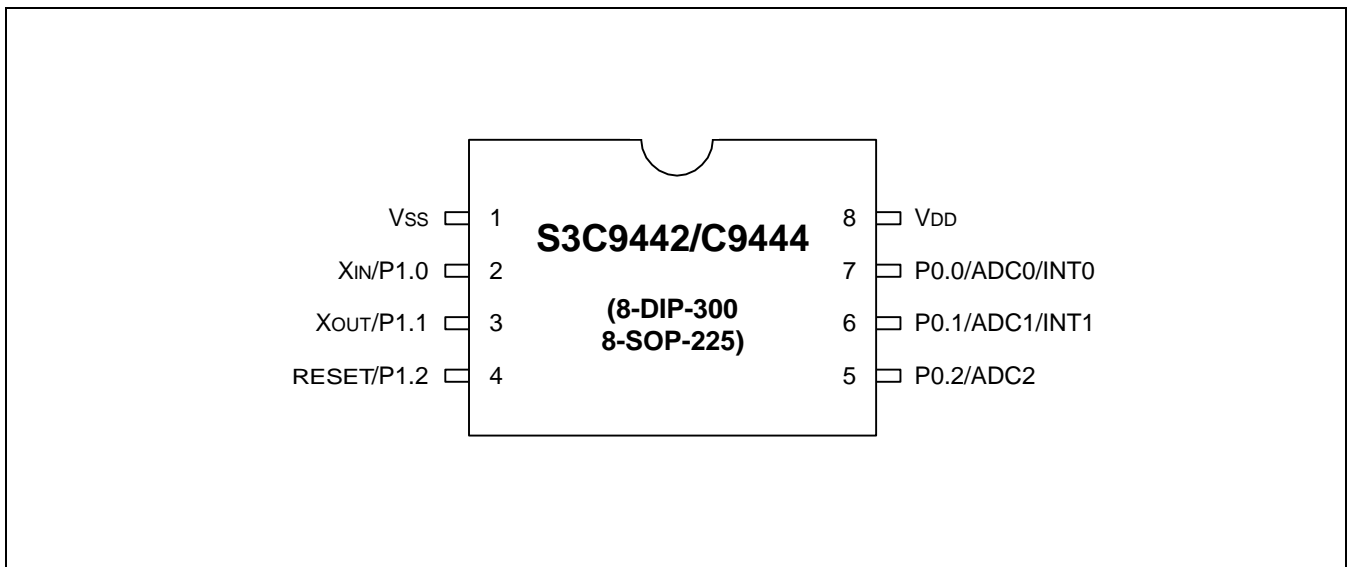


Figure 1-4. Pin Assignment Diagram (8-Pin DIP/SOP Package)

PIN DESCRIPTIONS

Table 1-1. S3C9452/C9454 Pin Descriptions

Pin Name	In/Out	Pin Description	Pin Type	Share Pins
P0.0–P0.7	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull output. Pull-up resistors are assignable by software. Port0 pins can also be used as A/D converter input, PWM output or external interrupt input.	E-1	ADC0–ADC7 INT0/INT1 PWM
P1.0–P1.1	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull, open-drain output. Pull-up resistors or pull-down resistors are assignable by software.	E-2	X_{IN} , X_{OUT}
P1.2	I	Schmitt trigger input port	B	RESET
P2.0–P2.6	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull, open-drain output. Pull-up resistors are assignable by software.	E E-1	– ADC8/CLO T0
X_{IN} , X_{OUT}	–	Crystal/Ceramic, or RC oscillator signal for system clock.		P1.0–P1.1
RESET	I	Internal LVR or External RESET	B	P1.2
V_{DD} , V_{SS}	–	Voltage input pin and ground		–
CLO	O	System clock output port	E-1	P2.6
INT0–INT1	I	External interrupt input port	E-1	P0.0, P0.1
PWM	O	8-Bit high speed PWM output	E-1	P0.6
T0	O	Timer0 match output	E-1	P2.0
ADC0–ADC8	I	A/D converter input	E-1 E	P0.0–P0.7 P2.6

PIN CIRCUITS

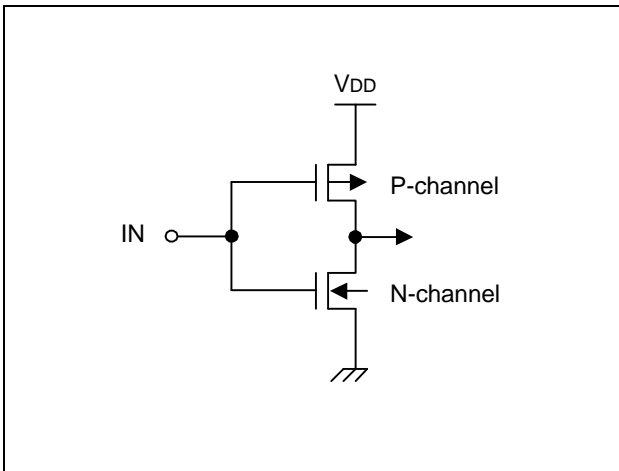


Figure 1-5. Pin Circuit Type A

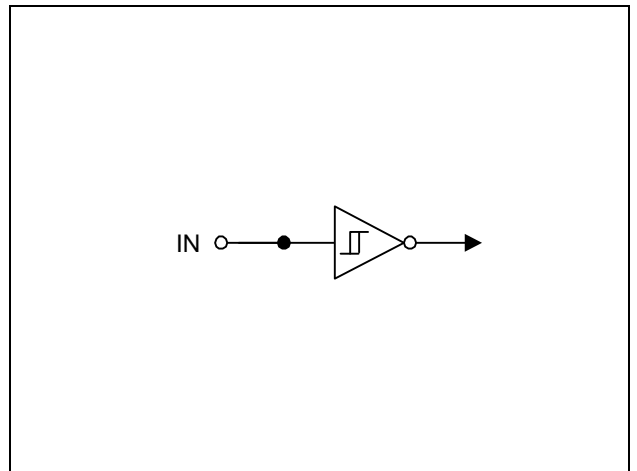


Figure 1-6. Pin Circuit Type B

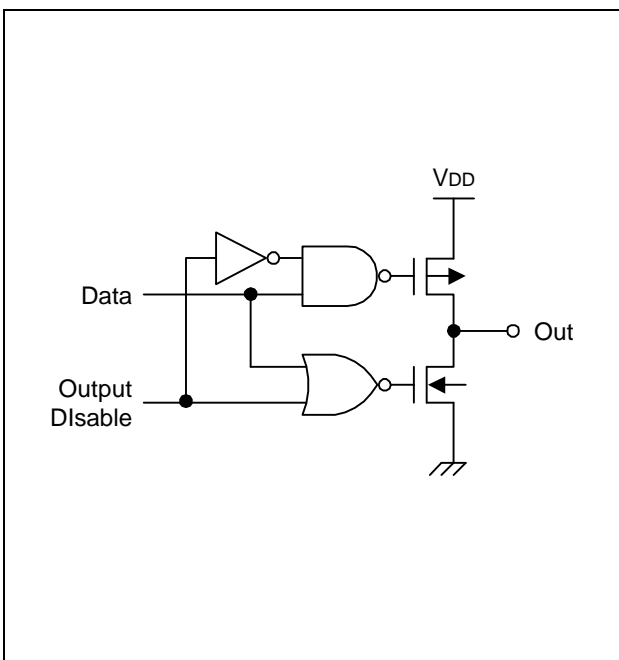


Figure 1-7. Pin Circuit Type C

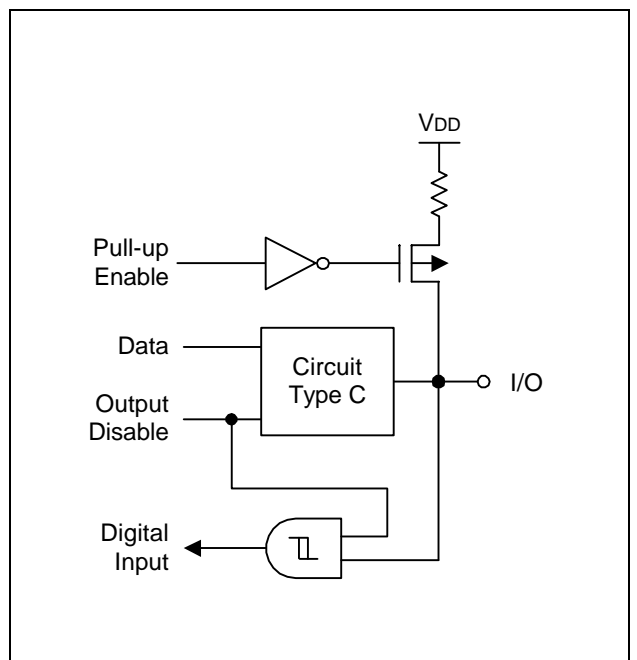


Figure 1-8. Pin Circuit Type D

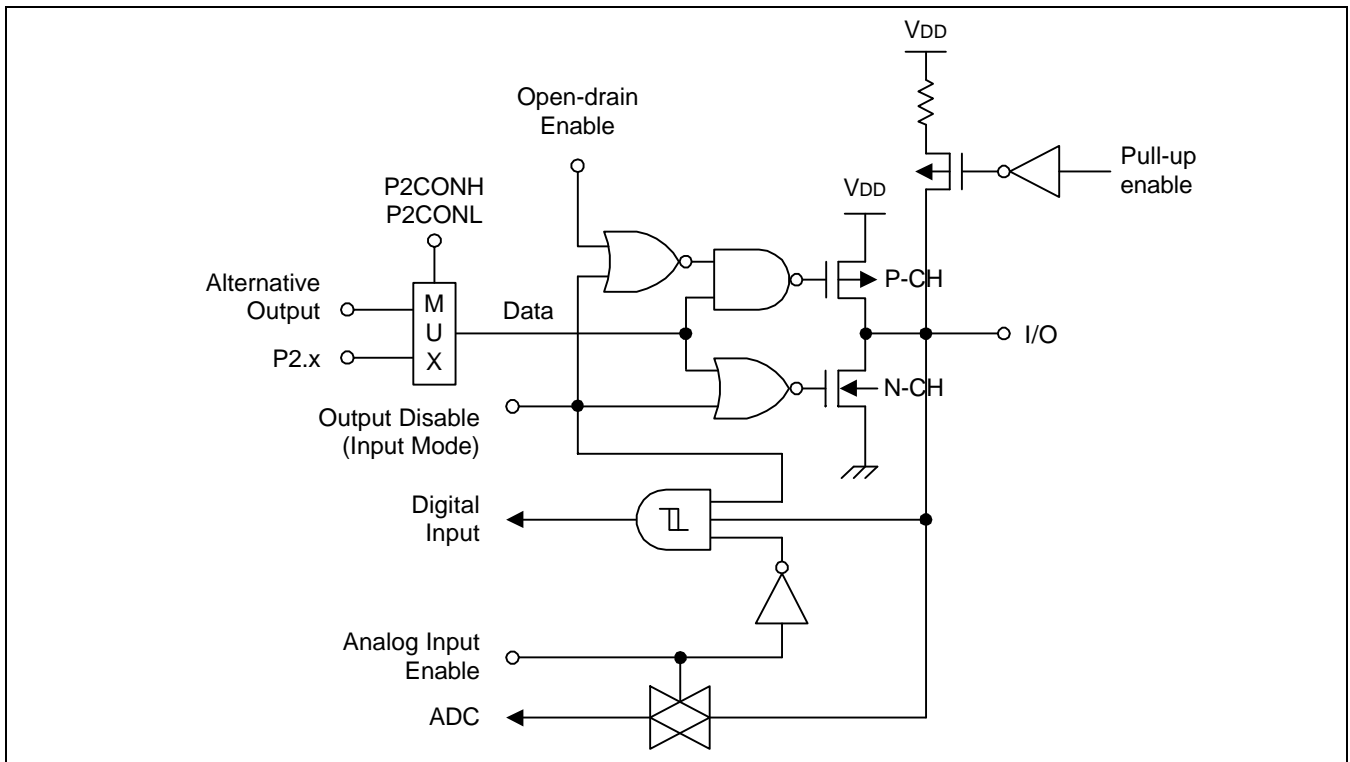


Figure 1-9. Pin Circuit Type E

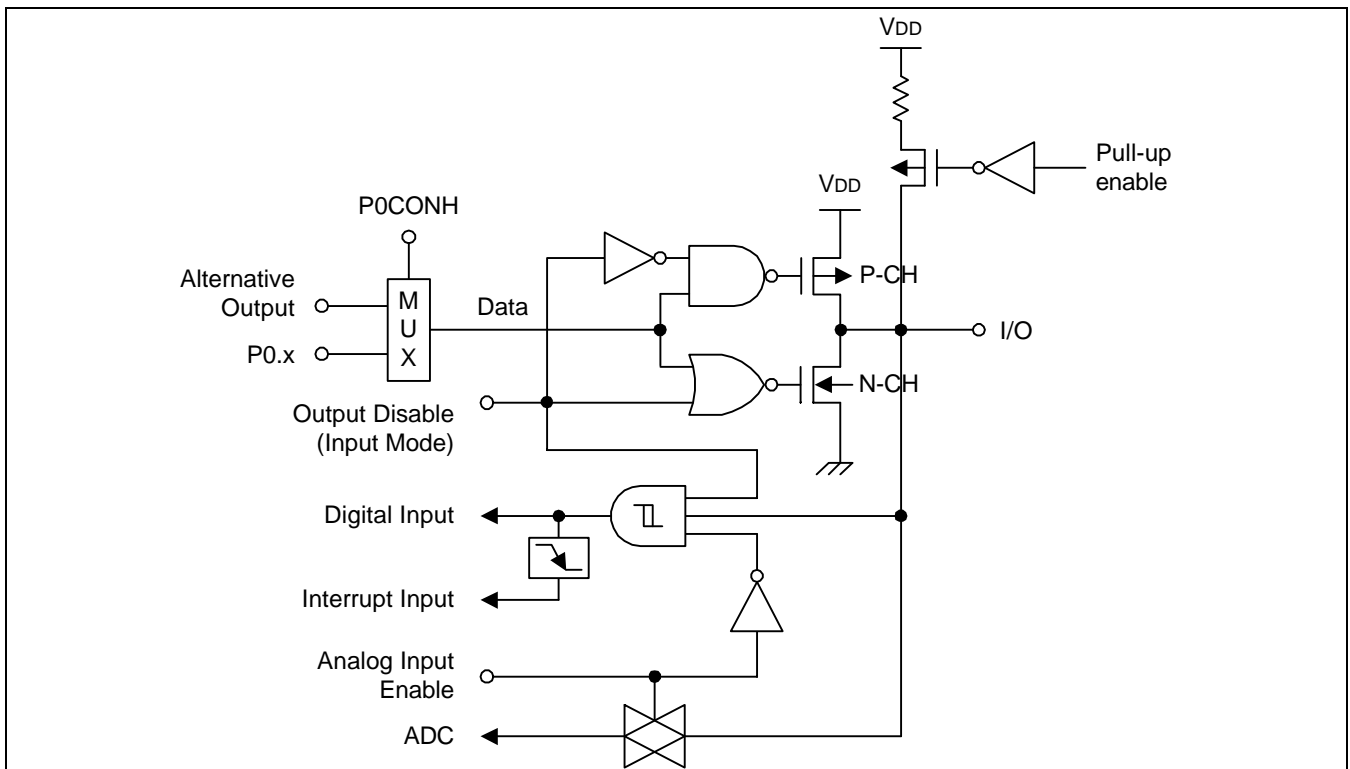


Figure 1-10. Pin Circuit Type E-1

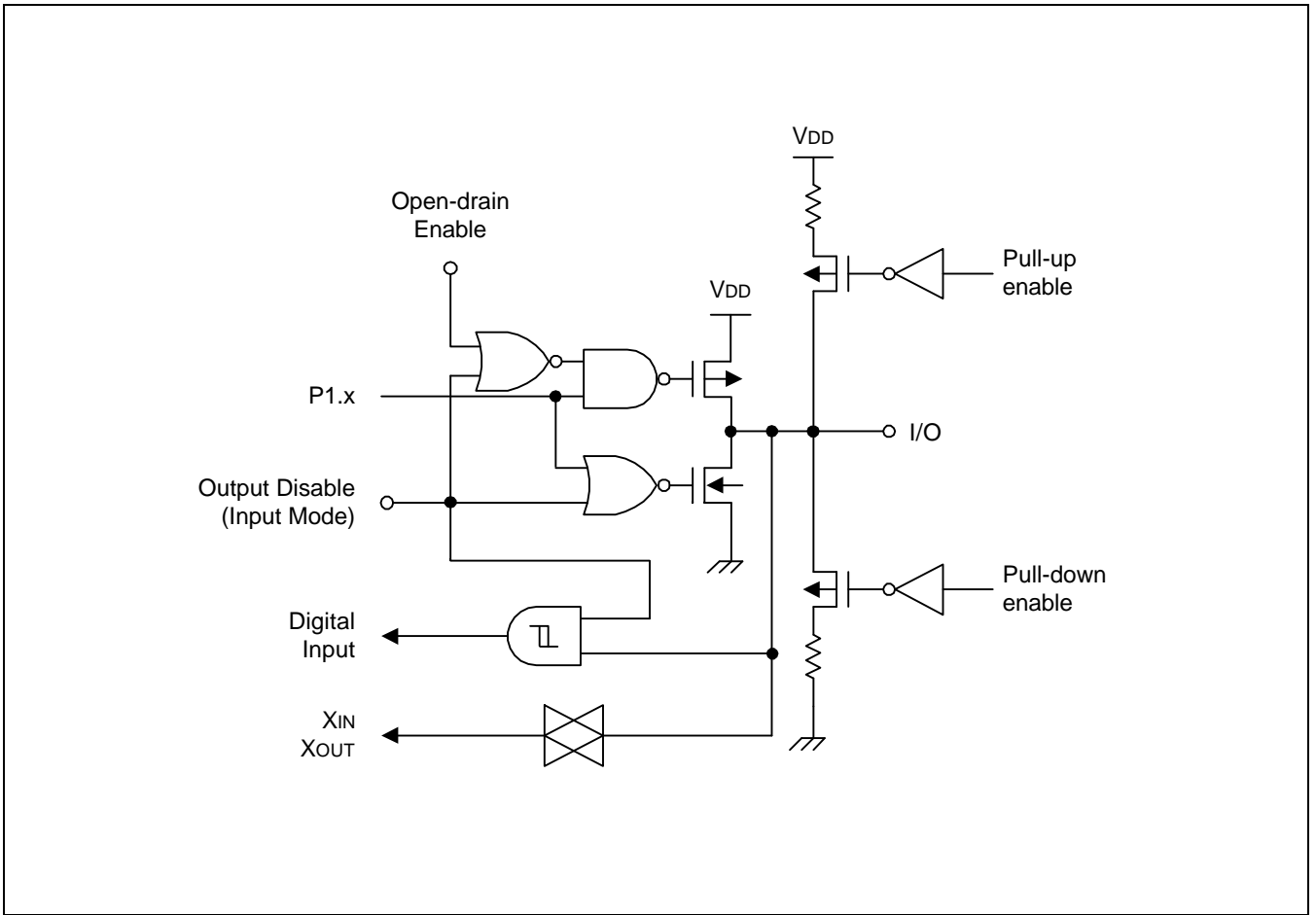


Figure 1-11. Pin Circuit Type E-2

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ELECTRICAL DATA

OVERVIEW

In this section, the following S3C9442/C9444/C9452/C9454 electrical characteristics are presented in tables and graphs:

- Absolute maximum ratings
- D.C. electrical characteristics
- A.C. electrical characteristics
- Input Timing Measurement Points
- Oscillator characteristics
- Oscillation stabilization time
- Operating Voltage Range
- Schmitt trigger input characteristics
- Data retention supply voltage in Stop mode
- Stop mode release timing when initiated by a RESET
- A/D converter electrical characteristics
- LVR circuit characteristics
- LVR reset Timing

Table 13-1. Absolute Maximum Ratings

 $(T_A = 25\text{ }^\circ\text{C})$

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input voltage	V_I	All ports	– 0.3 to $V_{DD} + 0.3$	V
Output voltage	V_O	All output ports	– 0.3 to $V_{DD} + 0.3$	V
Output current high	I_{OH}	One I/O pin active	– 25	mA
		All I/O pins active	– 80	
Output current low	I_{OL}	One I/O pin active	+ 30	mA
		All I/O pins active	+ 150	
Operating temperature	T_A	–	– 40 to + 85	$^\circ\text{C}$
Storage temperature	T_{STG}	–	– 65 to + 150	$^\circ\text{C}$

Table 13-2. DC Electrical Characteristics

 $(T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C, } V_{DD} = 2.0\text{ V to } 5.5\text{ V})$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	
Input high voltage	V_{IH1}	Ports 0, 1, 2 and RESET	$V_{DD} = 2.0\text{ to } 5.5\text{ V}$	$0.8 V_{DD}$	-	V_{DD}	V
	V_{IH2}	X_{IN} and X_{OUT}		$V_{DD} - 0.1$			
Input low voltage	V_{IL1}	Ports 0, 1, 2 and RESET	$V_{DD} = 2.0\text{ to } 5.5\text{ V}$	-	-	$0.2 V_{DD}$	V
	V_{IL2}	X_{IN} and X_{OUT}				0.1	
Output high voltage	V_{OH}	$I_{OH} = -10\text{ mA}$ ports 0, 1, 2	$V_{DD} = 4.5\text{ to } 5.5\text{ V}$	$V_{DD} - 1.5$	$V_{DD} - 0.4$	-	V
Output low voltage	V_{OL}	$I_{OL} = 25\text{ mA}$ port 0, 1, and 2	$V_{DD} = 4.5\text{ to } 5.5\text{ V}$	-	0.4	2.0	V
Input high leakage current	I_{LIH1}	All input except I_{LIH2}	$V_{IN} = V_{DD}$	-	-	1	μA
	I_{LIH2}	X_{IN} , X_{OUT}	$V_{IN} = V_{DD}$	-	-	20	
Input low leakage current	I_{LIL1}	All input except I_{LIL2} and RESET	$V_{IN} = 0\text{ V}$	-	-	-1	μA
	I_{LIL2}	X_{IN} , X_{OUT}	$V_{IN} = 0\text{ V}$	-	-	-20	
Output high leakage current	I_{LOH}	All output pins	$V_{OUT} = V_{DD}$	-	-	2	μA
Output low leakage current	I_{LOL}	All output pins	$V_{OUT} = 0\text{ V}$	-	-	-2	μA
Pull-up resistors	R_P	$V_{IN} = 0\text{ V}$ Ports 0, 1, 2	$V_{DD} = 5\text{ V}$	25	50	100	k Ω
Pull-down resistors	R_P	$V_{IN} = 0\text{ V}$ Ports 1	$V_{DD} = 5\text{ V}$	25	50	100	
Supply current	I_{DD1}	Run mode 10 MHz CPU clock	$V_{DD} = 4.5\text{ to } 5.5\text{ V}$	-	5	10	mA
		3 MHz CPU clock	$V_{DD} = 2.0\text{ V}$			2	
	I_{DD2}	Idle mode 10 MHz CPU clock	$V_{DD} = 4.5\text{ to } 5.5\text{ V}$	-	2	4	
		3 MHz CPU clock	$V_{DD} = 2.0\text{ V}$			0.5	
	I_{DD3}	Stop mode	$V_{DD} = 4.5\text{ to } 5.5\text{ V}$ (LVR disable)	-	0.1	5	
			$V_{DD} = 4.5\text{ to } 5.5\text{ V}$ (LVR enable)			100	
$V_{DD} = 2.6\text{ V}$ (LVR enable)			30			60	

NOTE: In STOP (I_{DD3}), IDLE (I_{DD2}) current, current by ADC module is not included.

Table 13-3. AC Electrical Characteristics

($T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $V_{DD} = 2.0\text{ V}$ to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt input low width	t_{INTL}	INT0, INT1 $V_{DD} = 5\text{ V} \pm 10\%$	–	200	–	ns
RESET input low width	t_{RSL}	Input $V_{DD} = 5\text{ V} \pm 10\%$	–	1	–	us

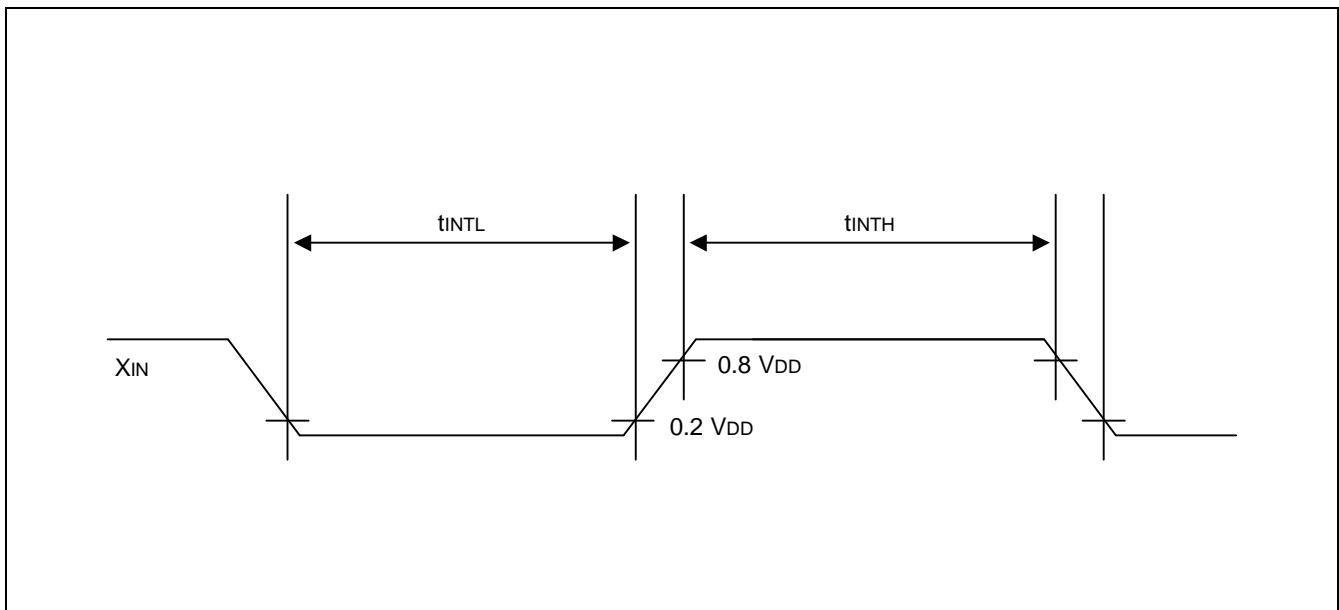


Figure 13-1. Input Timing Measurement Points

Table 13-4. Oscillator Characteristics

(T_A = -40°C to +85°C)

Oscillator	Clock Circuit	Test Condition	Min	Typ	Max	Unit
Main crystal or ceramic		V _{DD} = 4.5 to 5.5 V	1	-	10	MHz
		V _{DD} = 2.7 to 4.5 V	1	-	6	MHz
		V _{DD} = 2.0 to 2.7 V	1	-	3	MHz
External clock (Main System)		V _{DD} = 4.5 to 5.5 V	1	-	10	MHz
		V _{DD} = 2.7 to 4.5 V	1	-	6	MHz
		V _{DD} = 2.0 to 2.7 V	1	-	3	MHz
External RC oscillator	-	V _{DD} = 4.75 to 5.25 V Tolerance:10 %	-	4	-	MHz
Internal RC		V _{DD} = 4.75 to 5.25 V		3.2		
Oscillator				0.5		

Table 13-5. Oscillation Stabilization Time

(T_A = -40 °C to +85 °C, V_{DD} = 3.0 V to 5.5 V)

Oscillator	Test Condition	Min	Typ	Max	Unit
Main crystal	f _{OSC} > 1.0 MHz	-	-	20	ms
Main ceramic	Oscillation stabilization occurs when V _{DD} is equal to the minimum oscillator voltage range.	-	-	10	ms
External clock (main system)	X _{IN} input high and low width (t _{XH} , t _{XL})	25	-	500	ns
Oscillator stabilization	t _{WAIT} when released by a reset ⁽¹⁾	-	2 ¹⁶ /f _{OSC}	-	ms
wait time	t _{WAIT} when released by an interrupt ⁽²⁾	-	-	-	ms

NOTES:

- f_{OSC} is the oscillator frequency.
- The duration of the oscillator stabilization wait time, t_{WAIT}, when it is released by an interrupt is determined by the settings in the basic timer control register, BTCON.

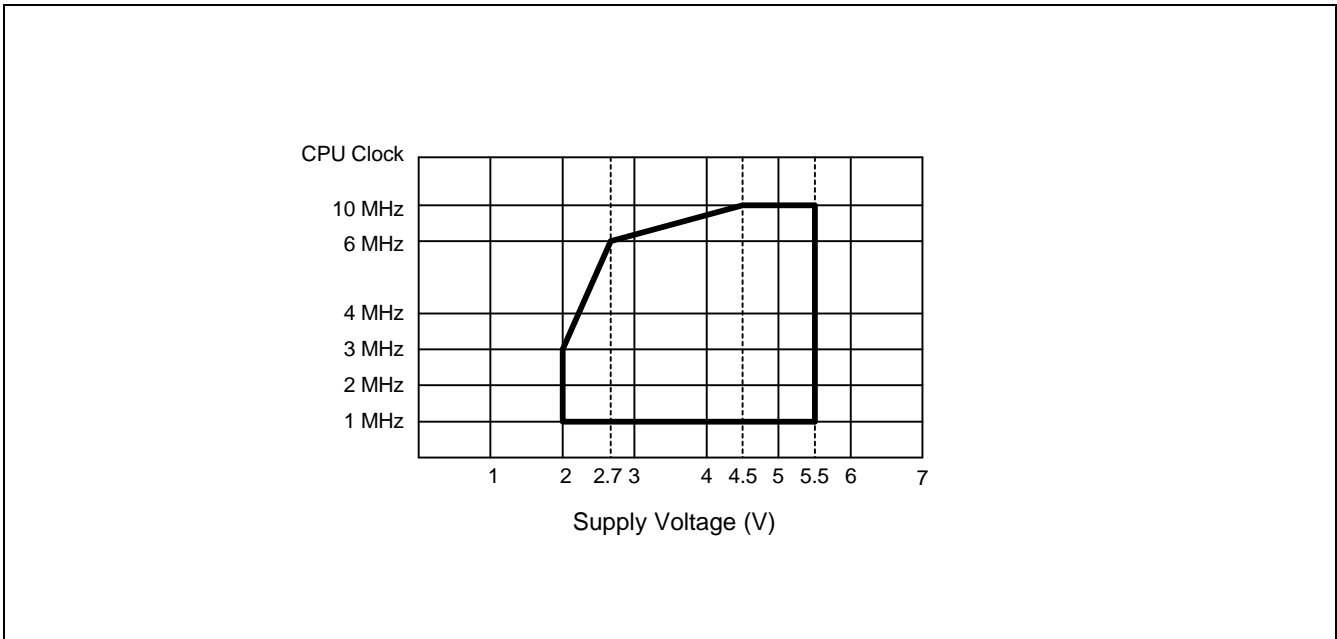


Figure 13-2. Operating Voltage Range

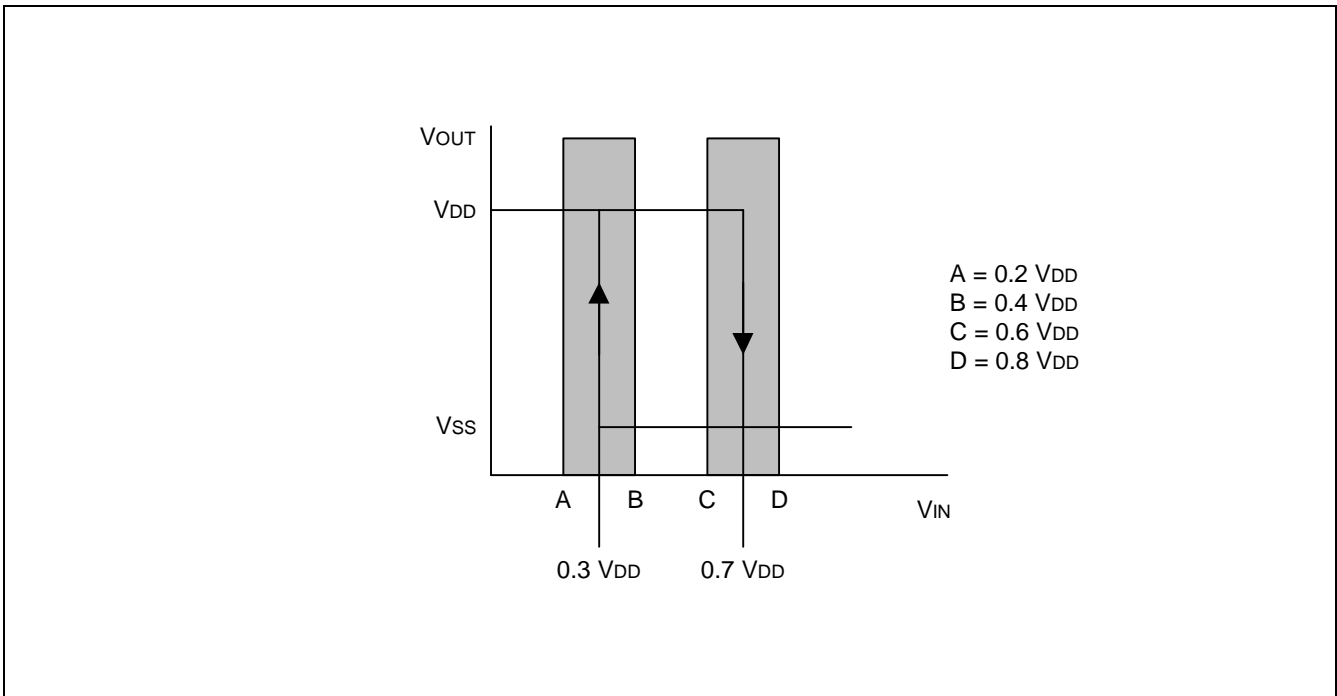


Figure 13-3. Schmitt Trigger Input Characteristics Diagram

Table 13-6. Data Retention Supply Voltage in Stop Mode

($T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $V_{DD} = 2.0\text{ V}$ to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	Stop mode	2.0	–	5.5	V
Data retention supply current	I_{DDDR}	Stop mode; $V_{DDDR} = 2.0\text{ V}$	–	0.1	5	μA

NOTE: Supply current does not include current drawn through internal pull-up resistors or external output current loads.

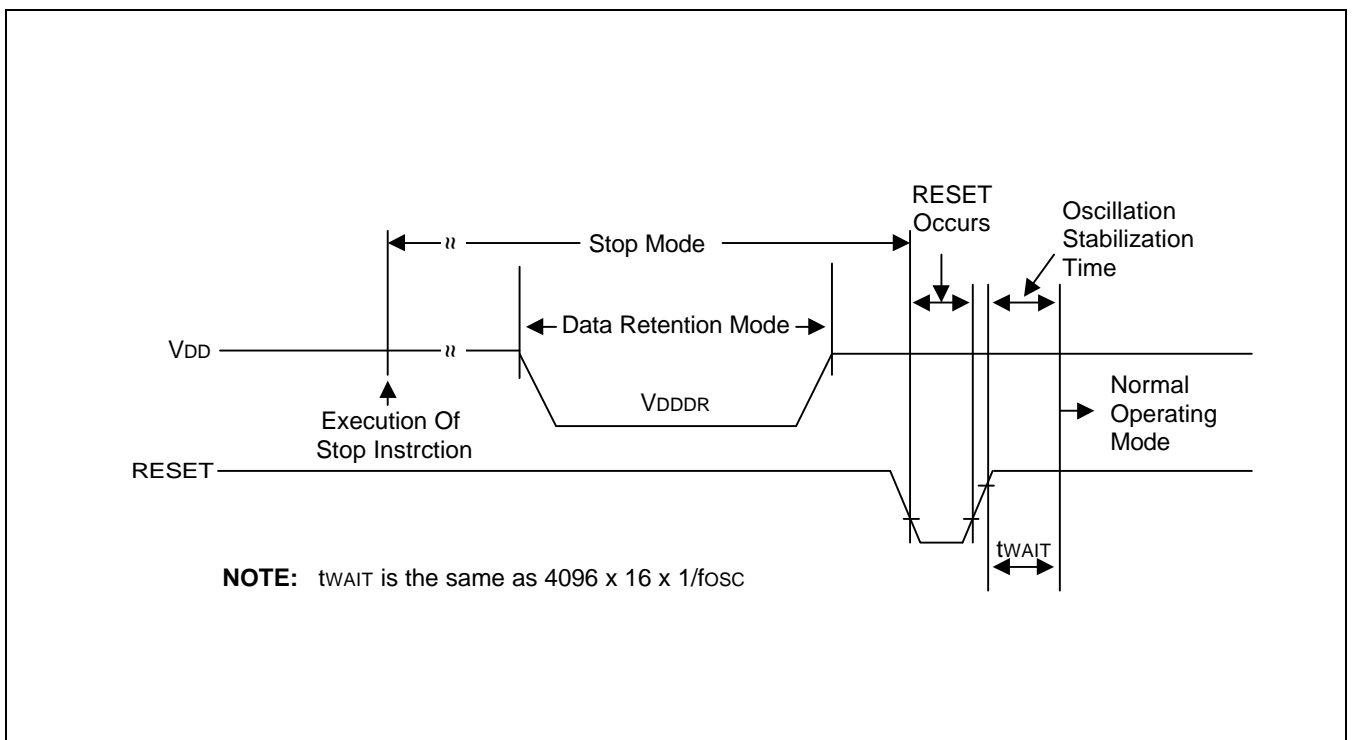


Figure 13-4. Stop Mode Release Timing When Initiated by a RESET

Table 13-7. A/D Converter Electrical Characteristics

(T_A = -40 °C to +85 °C, V_{DD} = 2.7 V to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Total accuracy	-	V _{DD} = 5.12 V CPU clock = 10 MHz V _{SS} = 0 V	-	-	± 3	LSB
Integral linearity error	ILE	"	-	-	± 2	
Differential linearity error	DLE	"	-	-	± 1	
Offset error of top	EOT	"	-	± 1	± 3	
Offset error of bottom	EOB	"	-	± 1	± 2	
Conversion time ⁽¹⁾	t _{CON}	f _{OSC} = 10 MHz	-	20	-	μs
Analog input voltage	V _{IAN}	-	V _{SS}	-	V _{DD}	V
Analog input impedance	R _{AN}	-	2	-	-	MΩ
Analog input current	I _{ADIN}	V _{DD} = 5 V	-	-	10	μA
Analog block current ⁽²⁾	I _{ADC}	V _{DD} = 5 V	-	1	3	mA
		V _{DD} = 3 V		0.5	1.5	
		V _{DD} = 5 V power down mode	-	100	500	nA

NOTES:

1. "Conversion time" is the time required from the moment a conversion operation starts until it ends.
2. I_{ADC} is operating current during A/D conversion.

Table 13-8. LVR Circuit Characteristics

(T_A = 25 °C, V_{DD} = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low voltage reset	V _{LVR}	–	–	2.3 3.0 3.9		V
LVR hysteresis voltage	V _{HYS}		–	0.3	–	V
Power supply voltage rise time	t _R		10		(note)	us
Power supply voltage off time	t _{OFF}		0.5			s

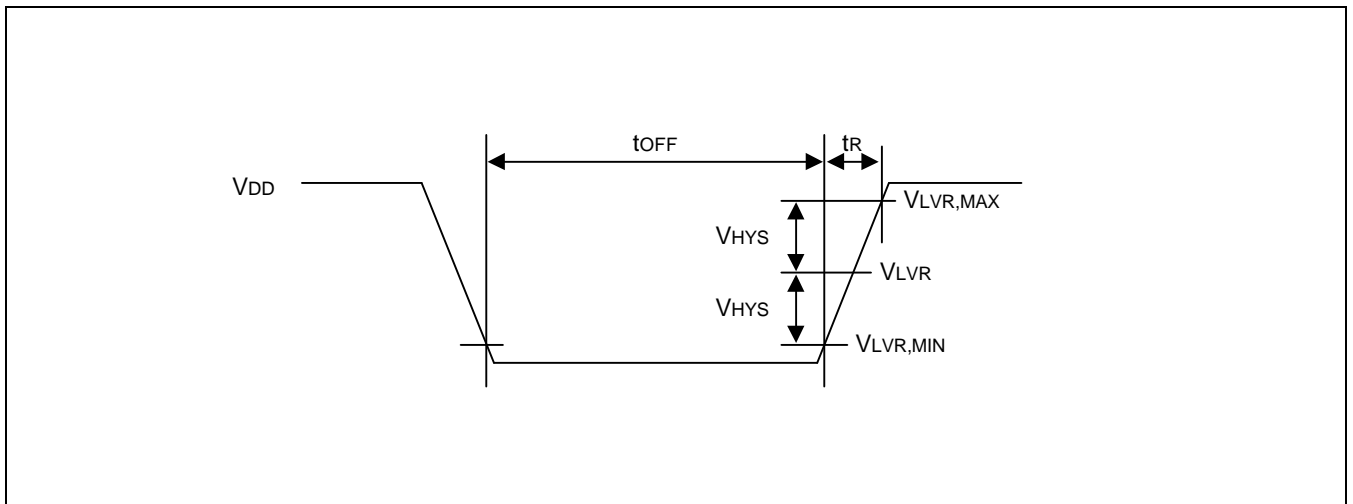
NOTE: $2^{16}/f_x$ (= 6.55 ms at $f_x = 10$ MHz)

Figure 13-5. LVR Reset Timing

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MECHANICAL DATA

OVERVIEW

The S3C9452/C9454 is available in a 20-pin DIP package (Samsung: 20-DIP-300A), a 20-pin SOP package (Samsung: 20-SOP-375), a 16-pin DIP package (Samsung: 16-DIP-300A). Package dimensions are shown in Figure 15-1, 15-2, and 15-3.

The S3C9442/C9444 is available in a 8-pin DIP package (SAMSUNG 8-DIP-300A), a 8-pin SOP package (SAMSUNG 8-SOP-225).

Package dimensions are shown in figure 14-4 and 14-5.

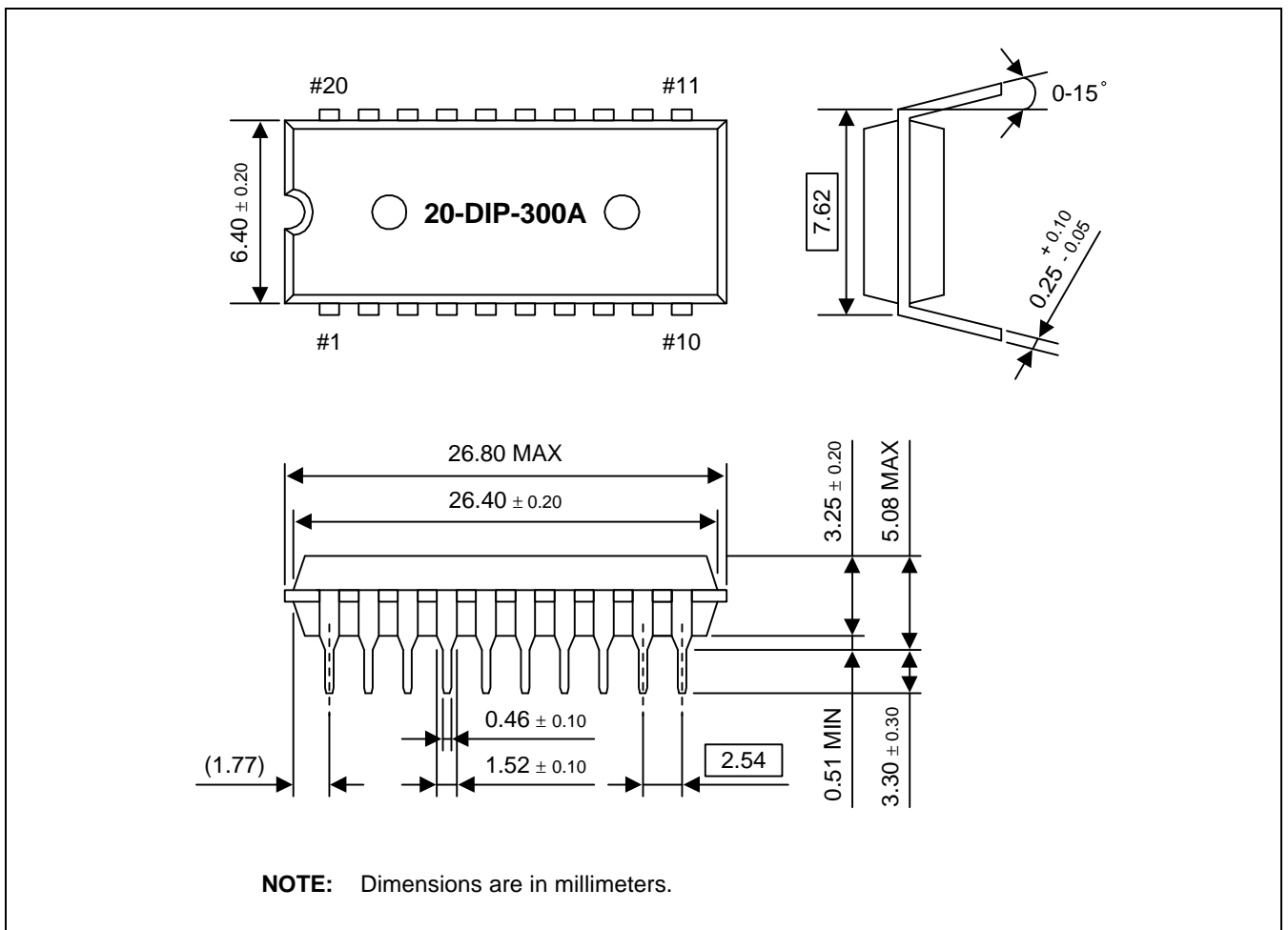


Figure 14-1. 20-DIP-300A Package Dimensions

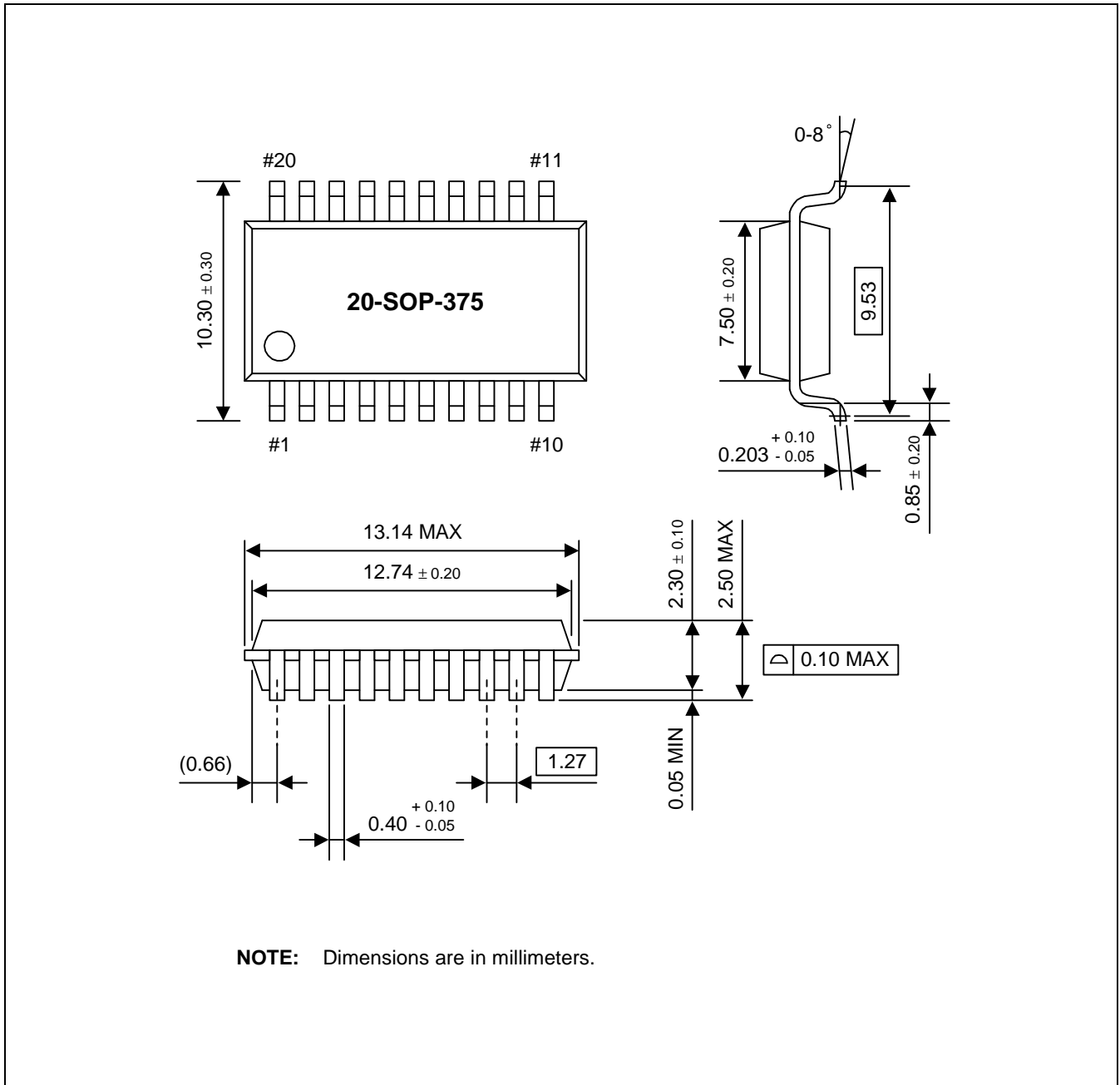


Figure 14-2. 20-SOP-375 Package Dimensions

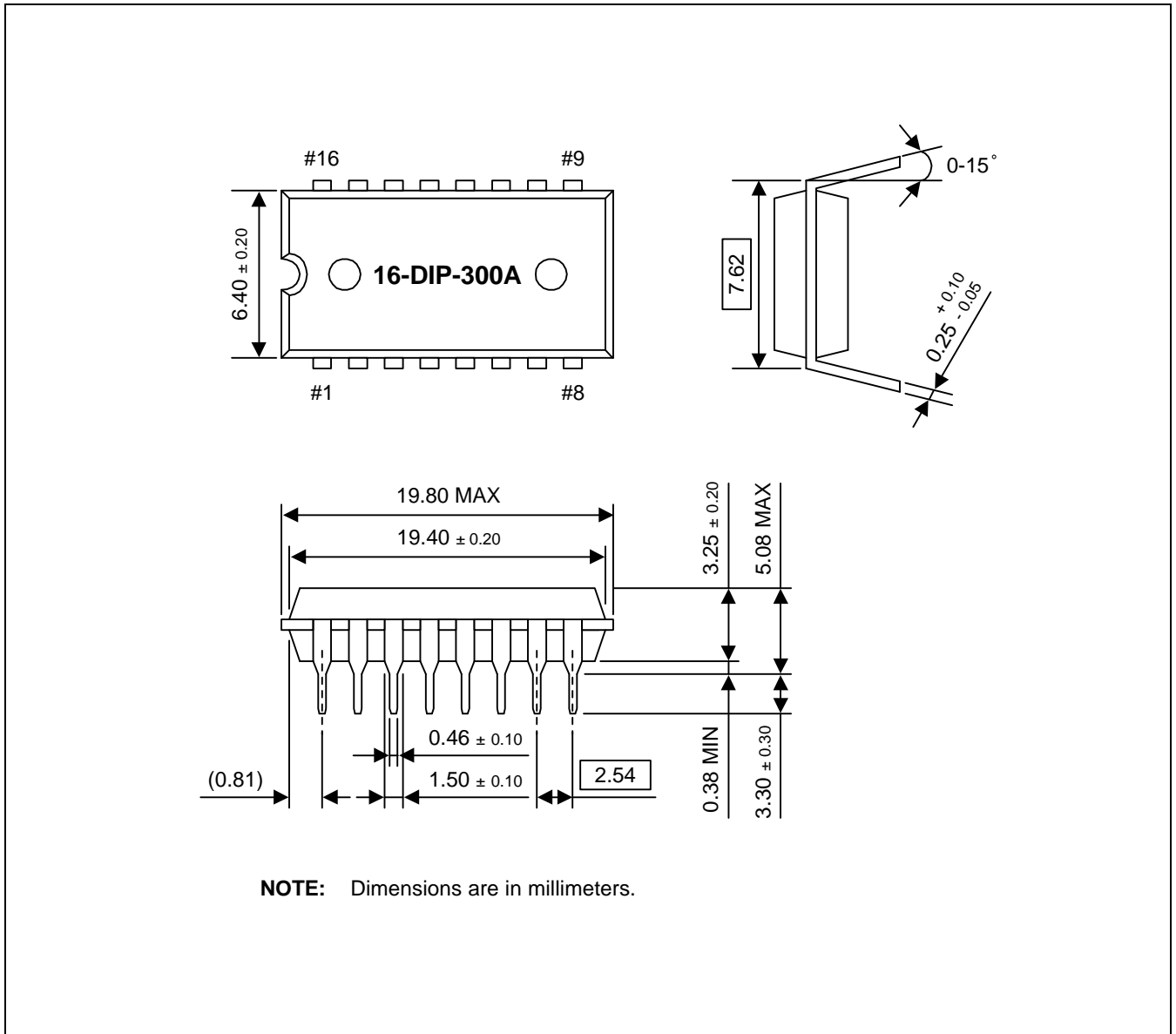
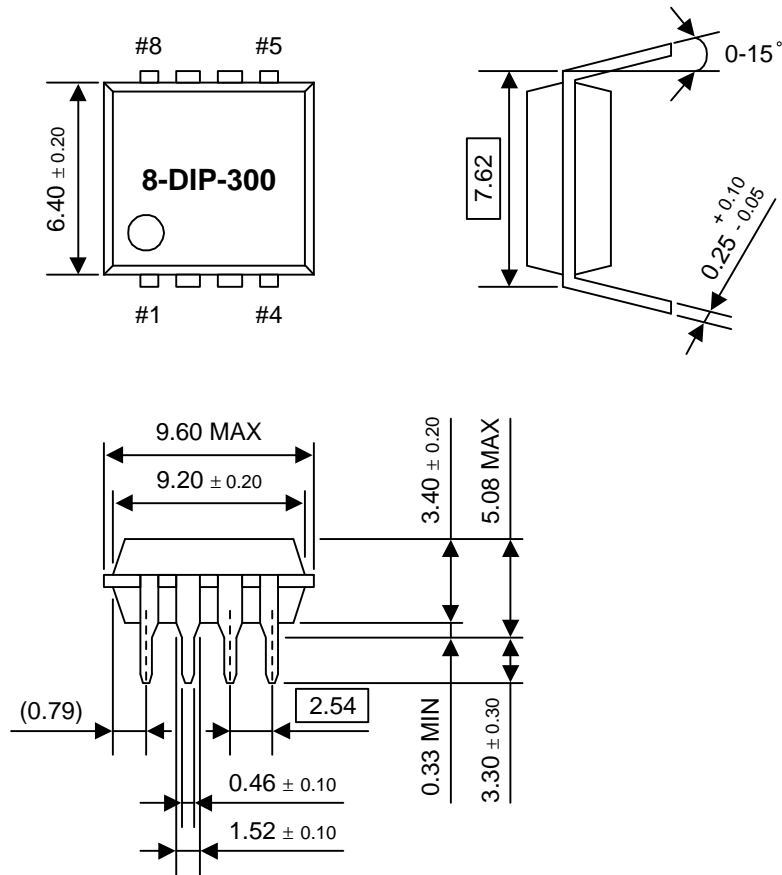
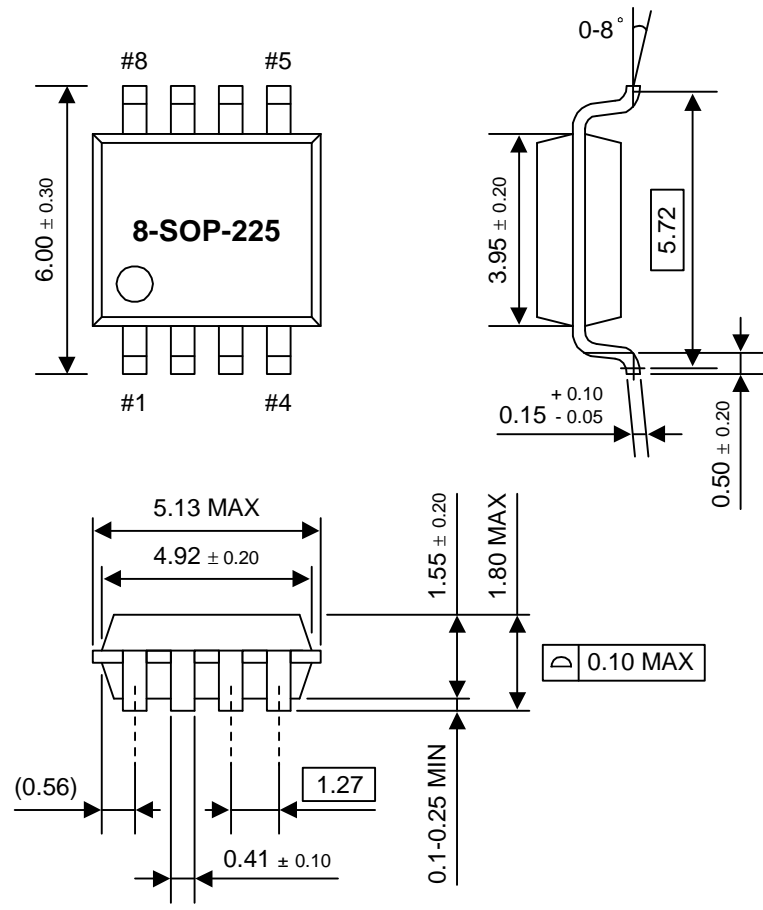


Figure 14-3. 16-DIP-300A Package Dimensions



NOTE: Dimensions are in millimeters.

Figure 14-4. 8-DIP-300 Package Dimensions



NOTE: Dimensions are in millimeters.

Figure 14-5. 8-SOP-225 Package Dimensions

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S3F9444/F9454 MTP

OVERVIEW

The S3F9444/F9454 single-chip CMOS microcontroller is the MTP (Multi Time Programmable) version of the S3C9442/C9444/C9452/C9454 microcontroller. It has an on-chip Flash ROM instead of masked ROM. The Flash ROM is accessed by serial data format.

The S3F9444/F9454 is fully compatible with the S3C9442/C9444/C9452/C9454, in function, in D.C. electrical characteristics, and in pin configuration. Because of its simple programming requirements, the S3F9444/F9454 is ideal for use as an evaluation chip for the S3C9442/C9444/C9452/C9454.

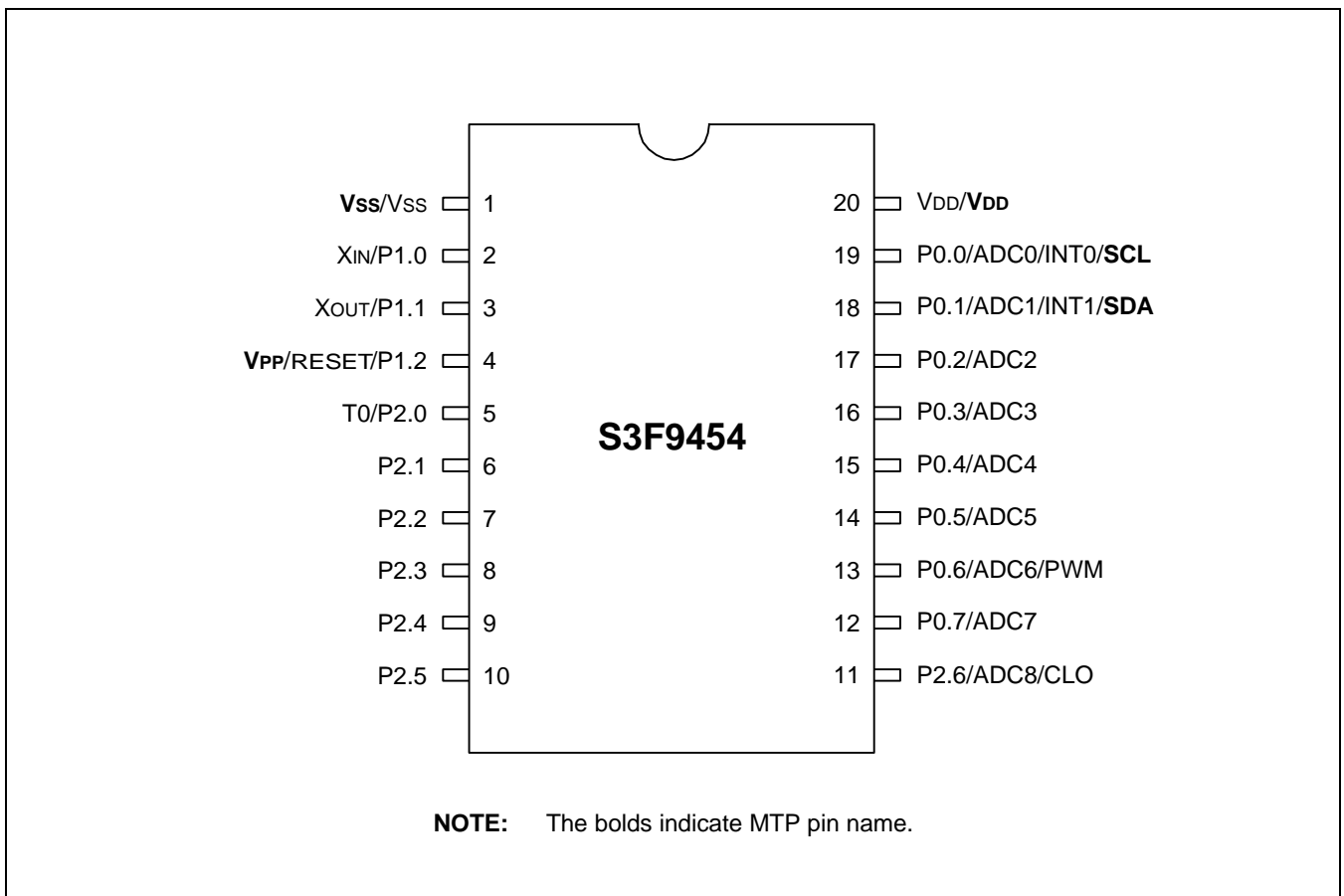


Figure 15-1. Pin Assignment Diagram (20-Pin Package)

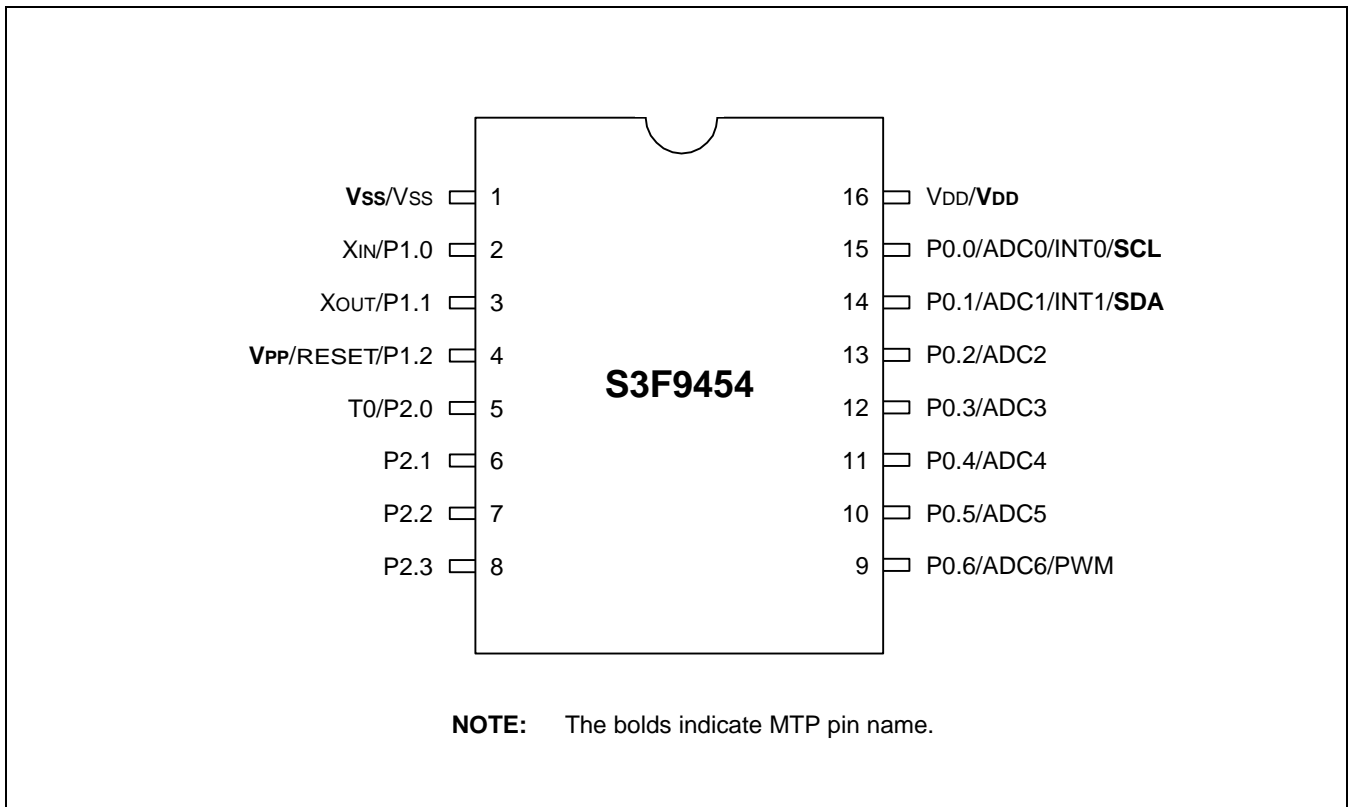


Figure 15-2. Pin Assignment Diagram (16-Pin Package)

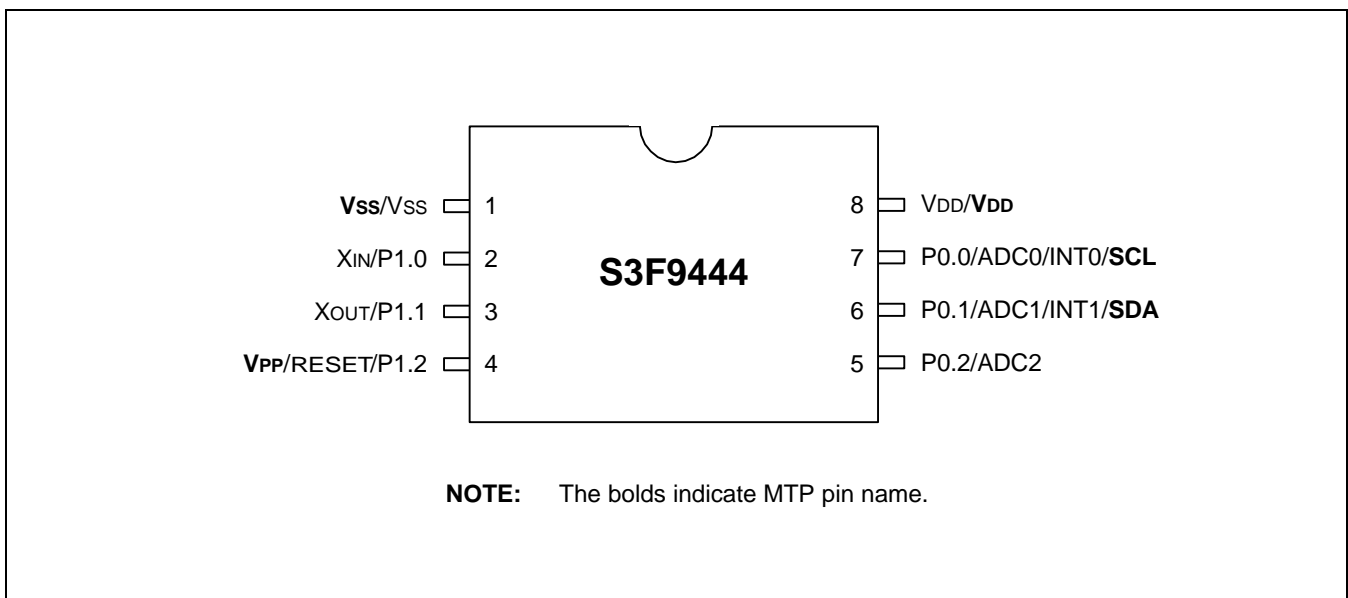


Figure 15-3. Pin Assignment Diagram (8-Pin Package)

Table 15-1. Descriptions of Pins Used to Read/Write the Flash ROM

Main Chip Pin Name	During Programming			
	Pin Name	Pin No.	I/O	Function
P0.1	SDA	18 (20-pin) 14 (16-pin)	I/O	Serial data pin (output when reading, Input when writing) Input and push-pull output port can be assigned
P0.0	SCL	19 (20-pin) 15 (16-pin)	I	Serial clock pin (input only pin)
RESET, P1.2	V _{PP}	4	I	Power supply pin for flash ROM cell writing (indicates that MTP enters into the writing mode). When 12.5 V is applied, MTP is in writing mode and when 5 V is applied, MTP is in reading mode. (Option)
V _{DD} /V _{SS}	V _{DD} /V _{SS}	20 (20-pin), 16 (16-pin) 1 (20-pin), 1 (16-pin)	I	Logic power supply pin.

Table 15-2. Comparison of S3F9444/F9454 and S3C9442/C9444/C9452/C9454 Features

Characteristic	S3F9444/F9454	S3C9442/C9444/C9452/C9454
Program Memory	4 Kbyte Flash ROM	2K/4K byte mask ROM
Operating Voltage (V _{DD})	2.0 V to 5.5 V	2.0 V to 5.5 V
OTP Programming Mode	V _{DD} = 5 V, V _{PP} = 12.5 V	
Pin Configuration	20 DIP/20 SOP/16 DIP/8 DIP/8 SOP	
EPROM Programmability	User Program multi time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP} pin of the S3F9444/F9454 Flash ROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 15-3 below.

Table 15-3. Operating Mode Selection Criteria

V _{DD}	V _{PP}	REG/MEM	Address (A15–A0)	R/W	Mode
5 V	5 V	0	0000H	1	Flash ROM read
	12.5 V	0	0000H	0	Flash ROM program
	12.5 V	0	0000H	1	Flash ROM verify
	12.5 V	1	0E3FH	0	Flash ROM read protection

NOTE: "0" means Low level; "1" means High level.